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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,317	11/14/2001	Yohei Akita	HITA.0123	6888

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REED SMITH LLP
3110 FAIRVIEW PARK DRIVE, SUITE 1400
FALLS CHURCH, VA 22042

EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 05/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/987,317	AKITA, YOHEI	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been presented for examination based on applicant's disclosure filed on 14 November 2001. Claims 1-20 have been rejected by the examiner.

Drawings

2. Applicant's drawings submitted on 14 November 2001 have been approved by the examiner.

Priority

3. Applicants claim for foreign priority based on Japanese application number 2000-348349 filed 15 November 2000 is acknowledged. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. *The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to*

which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Specifically, claim 3, recites a limitation relating to a "fabrication means" that has not been sufficiently disclosed in the specification. While the specification makes reference in very general terms to "the fabrication 153 of the LSI is carried out" (page 27, line 3), there is no sufficient teaching that would allow a skilled artisan to realize the claimed limitation from the description given in the specification. There are no specific methods, techniques, or models disclosed for actually implementing the "fabrication means" sufficient to allow one skilled in the art to make and use the claimed subject matter without undue experimentation. Further, no flow charts or figures have been provided which demonstrate the claimed fabrication means are disclosed. The examiner therefore submits that the specification does not provide a clear and concise description of the subject matter claimed in dependent claim 3.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-15, and 18-19 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,446,243 issued to Huang et al.

Regarding independent claim 1: Huang teaches a system verification method for verifying the operation of system design modules (CL4-L29-28, Figs. 4-6) that are protected as intellectual property (CL3-L21, CL4-L33) inclusive of providing design data for a verification module (CL4-L38-42, Fig. 2), simulating system operation to obtain an output (CL4-L38-42, Fig. 4), supplying input vectors to modules (CL4-47, 56-64, Fig. 4), computing output vectors based on a verification module (CL4-L38-42, Fig. 2), integrating output vectors (CL4-L43-54) , and repeating. Further, since it is well established that logic simulators perform synchronous operations (i.e. Verilog type, CL4-L61) when simulating a circuit design that are based on time steps, the claimed limitations relating to dividing the simulation into a number of time steps, and performing the input/output operations within a particular time step, would obviously be inherent in the prior art. Also, the warning messages (CL6-L54, Fig. 10) disclosed by Huang serve to "transmit" module verification vectors to an outside entity, and are hence functionally equivalent to the limitations relating to the claimed "transmitting of an input vector" of the claimed invention.

Regarding independent claims 2 and 7: As noted above, Huang teaches a system verification method, means, and equipment for verifying the operation of system design modules (CL4-L29-28, Figs. 4-6) that are protected as intellectual property (CL3-L21, CL4-L33) inclusive of providing design data for a verification module (CL4-L38-42, Fig. 2), simulating system operation to obtain an output (CL4-L38-42, Fig. 4), supplying input vectors to modules (CL4-47, 56-64, Fig. 4), computing output vectors based on a verification module (CL4-L38-42, Fig. 2), integrating output vectors (CL4-L43-54) , and

repeating. Huang therefor includes the functional "means" for simulating the system (CL4-L38-42, Fig. 4), supplying means and receiving means for input vectors (CL4-47, 56-64, Fig. 4), integrating means and computing means for output vectors (CL4-L43-54), and repeating means. As also previously noted above, the warning messages (CL6-L54, Fig. 10) disclosed by Huang serve to "transmit" module verification vectors, and hence provide a transmitting means to an outside entity.

Regarding dependent claims 3: Huang discloses a fabricating means for a integrated circuit (Fig. 1, 20).

Regarding dependent claims 4-5, 8-12, 18-19: Huang discloses a computer-implemented apparatus (CL3-L 17) for implementing the IP core and logic simulator that would inherently include a communications line for exchange of information over the internet or via a leased line. Further, it is well established that communication over the internet inherently provides a data encryption and authentication means.

Regarding dependent claim 6: Huang teaches single chip SoC design (CL1-L51).

Regarding dependent claims 13-14: Huang discloses detecting the occurrence of a violation (i.e. illegal use) of the design intention during verification (CL6-L60-64).

Regarding dependent claim 15: Huang teaches an analyzing means for monitoring vector sequences (CL3-L31-44).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 16-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,446,243 issued to Huang et al in view of U.S. Patent 6,782,511 issued to Frank et al.

Regarding claims 16-17: As previously cited above, Huang renders obvious the limitations of independent claim 7 relating to a system verification method, means, and equipment for verifying the operation of a system design modules (CL4-L29-28, Figs. 4-6) that are protected as intellectual property (CL3-L21, CL4-L33).

Huang does not explicitly disclose the use of a service charge means in for protected intellectual property in a system design.

Frank teaches a behavioral model simulation tool hosted privately on the webserver tests and validates the system design. The simulation tool executes only in the secure environment of the business-to-business application service provider. The validated solution is then downloaded back over the Internet (i.e. third party) for a pay-per-use fee (i.e. service charge) to the customer (CL2-L1-7).

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Huang relating to a system verification method, means, and equipment for verifying the operation of system design modules that are protected as intellectual property, with the teachings of Frank relating to validated design solution downloading over the Internet and a pay-per-use fee (i.e. service charge) to the customer, to realize the claimed invention. An obvious motivation exists since, in this case, the Huang reference teaches to the Frank reference, and the Frank reference teaches to the Huang reference. Specifically, both Huang and Frank teach verification of simulated system designs of protected intellectual property and are used in the same technological arena as noted above. Huang teaches to Frank because Huang teaches verifying the operation of a system design modules including input/output vectors and integration (See: Huang, Summary of Invention). Frank teaches to Huang because Frank specifically teaches validated design solution downloading over the Internet and a pay-per-use fee (i.e. service charge). (See: Frank: Abstract/Summary) Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Huang/Frank, Background/Abstract) Accordingly, a skilled artisan having access to the teachings of Huang and Frank, would have knowingly modified the teachings of Huang with the teachings of Frank (or visa versa) to realize the claimed elements of the present invention while reducing the cost and development time.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,157,947 issued to Watanable et al teaches system verification of a system design modules that are protected as intellectual property.

U.S. Patent 6,687,710 issued to Dey teaches system verification of a system design modules that are protected as intellectual property.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

Fred Ferris, Patent Examiner
Simulation and Emulation, Art Unit 2128
U.S. Patent and Trademark Office
Randolph Building, Room 5D19
401 Dulany Street
Alexandria, VA 22313
Phone: (571-272-3778)
Fred.Ferris@uspto.gov
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